Development of low-power data logger for earthquake observation

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We are developing a small,light and low-power data logger which is chiefly for extra observations of earthquakes.Because the logger which has good mobility and can work for a long time by itself is useful to reduce efforts of people who would have to go to the observation point where is inconvenient to go again and again to change a battery and so on,without it.In this study,we reduce electricity power consumption by not only making the circuit with low-power ICs but also change the system from the conventional one.In our way CPU and our original sequential circuit share tasks which control the logger while only CPU controls the logger in the conventional way because the sequential circuit can prevent the logger from wasting the power.The faster IC works,the more power it consumes.If CPU controlled sampling of analog signals from the seismometer whose rate is much lower than its working speed,it would have to wait for the next sampling timing for a relatively long time and waste the power because it works fast even though it doesn't anything.So we have made the sequential circuit which works much slower than CPU and had it controlling sampling instead of CPU.CPU can sleep at almost all times and only has to work when it sends all data which are sampled and temporarily saved in SRAM to the huge capacity recording media once a few minutes.In our system both reducing the power and making use of CPU's high speed are possible.And it is also possible to continue sampling whithout any break by using 2 SRAMs.Now we are developing the logger based on our idea,using PIC as PIC.The logger hasn't been completed yet.But during 100Hz

,16bit,1channel sampling by using the sequential circuit and ADS 7807 as A/D converter ,the power consumption is about 15 mW,which is less than one tenth value of any other loggers.