Japan Geoscience Union Meeting 2010
(May 23-28 2010 at Makuhari, Chiba, Japan)

PEM030-P06 Room: Convention Hall Time: May 26 17:15-18:45

Development of Miniaturized Sweep Frequency Analyzer using ASIC

Hajime Fukuhara[1*], Hirotsugu Kojima[2], Hirokazu Ikeda[3], Hiroshi Yamakawa[2]

[1]Kyoto Univ. EE, [2]Kyoto Univ. RISH, [3]JAXA/ISAS

A sweep frequency analyzer (SFA) is a part of plasma wave receivers to observe plasma waves in wide frequencies. The SFA is basically a heterodyne receiving system with low noises and high frequency resolution. The SFA has a PLL, which is frequency synthesizer. It takes several seconds to sweep all range. Since the total time to lock in all frequencies is not short enough in PLL, the SFA generally has disadvantage in temporal resolution. We propose a new kind of the SFA combined with FFT in FPGA (Field Programmable Gate Array). To improve the temporal resolution, sweep steps are widened and number of the steps is decreased. The bandwidth brought out of the heterodyne receiver is also widened. Observed signals are converted into digital signals and input to the FPGA. The FPGA has logic FFT blocks and apply the FFT to the digital signals. Thus, we can obtain the frequency resolution which is equals to the widened bandwidth divided by the FFT points. For example, we assume the sweep steps become tem times and the number of steps becomes tenth. Applying 64-point FFT in the FPGA, the temporal and frequency resolutions are respectively improved up to ten times and six times. We achieve high temporal resolution in the SFA without frequency resolution dropping. We have developed several analog circuits in the new SFA, such as PLL, and band pass filters using ASIC (Application Specific Integrated Circuit) technology. The ASIC technology enables extreme miniaturization of analog circuits. There is possibility to realize the analog circuits of the SFA in a chip of 5 mm x 5mm. We introduce the new SFA and development of the required circuits.

Keywords: Plasma Wave Receiver, Sweep Frequency Analyzer, ASIC, Miniaturization